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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,199	09/08/2003	Kazuhisa Nakata	60188-646	7483
7590	02/24/2005			
Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY 600 Thirteenth Street, N.W. Washington, DC 20005-3096			EXAMINER CAO, PHAT X	
			ART UNIT 2814	PAPER NUMBER

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.	Applicant(s)
10/656,199	NAKATA ET AL.
Examiner	Art Unit
Phat X. Cao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

1) Responsive to communication(s) filed on 12 November 2004.  
2a) This action is FINAL. 2b) This action is non-final.  
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.  
4a) Of the above claim(s) 3-5 and 9-11 is/are withdrawn from consideration.  
5) Claim(s) \_\_\_\_\_ is/are allowed.  
6) Claim(s) 1 is/are rejected.  
7) Claim(s) 2 and 6-8 is/are objected to.  
8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

9) The specification is objected to by the Examiner.  
10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

1) Notice of References Cited (PTO-892)  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_  
5) Notice of Informal Patent Application (PTO-152)  
6) Other: \_\_\_\_\_

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election of Group III (claims 1,2, 6, 7, and 8) in the reply filed on 11/12/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

***Specification***

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

***Claim Objections***

3. Claims 6-7 are objected to because of the following informalities:

- in claim 6, lines 6-7, "wherein gates of nMISFETs of the first type are arranged in the second discontinuous active region" should be changed to "wherein **the gate of an nMISFET** of the first type **is** arranged in the second discontinuous active region".

- in claim 6, lines 7-9, "whereas a gate of an nMISFET of the second type, which needs higher current driving capability than the nMISFETs of the first type, is placed in the second continuous active region" should be changed to "whereas **gates of nMISFETs** of the second type, which **need** higher current driving capability than **the nMISFET** of the first type, **are** placed in the second continuous active region".

- in claim 7, lines 7-8, "wherein gates of nMISFETs of a first type are arranged in the discontinuous active region" should be changed to "wherein **the gate of an nMISFET** of a first type **is** arranged in the discontinuous active region".

- in claim 7, lines 8-10, "whereas a gate of an nMISFET of a second type, which needs higher current driving capability than the nMISFETs of the first type, is placed in the continuous active region" should be changed to "whereas **gates** of nMISFETs of a second type, which **need** higher current driving capability than the nMISFET of the first type, **are** placed in the continuous active region".

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Inaba et al (US. 6,448,618).

Inaba (Fig. 1) discloses a semiconductor device comprising: a first discontinuous

active region 11b in which only a gate of a pMISFET is placed (column 7, lines 52-54); a first continuous active region 11a in which gates of three or more respective pMISFETs are arranged (column 7, lines 52-54); and a trench isolation 12 surrounding the first discontinuous active region 11b and the first continuous active region 11a, wherein gates of pMISFETs of a first type are arranged in the first continuous active region 11a, whereas a gate of a pMISFET of a second type, which needs higher current driving capability than the pMISFETs of the first type, is placed in the first discontinuous active region 11b (column 7, lines 43-47).

***Allowable Subject Matter***

6. Claims 2 and 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- the prior art of record fails to disclose the structure and characteristics of the two respective MISFETs disposed in the two-input active region as claimed in claims 2 and 8.

- The prior art of record fails to disclose the gates of nMISFETs placed in the continuous active region having higher current driving capability than the gate of an nMISFET disposed in the discontinuous active region as claimed in claims 6 and 7.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC  
February 18, 2005



PHAT X. CAO  
PRIMARY EXAMINER